WHAT IS CLAIMED IS:

1. A rapidly driving liquid crystal display, comprising:

a liquid crystal panel having a plurality of pixels;

a timing control circuit for issuing a gate clock signal and a plurality of control signals;

a gray voltage generation circuit for generating a plurality of gray voltages corresponding to data to be displayed in the panel in response to the gate clock signal;

a gate driving circuit for sequentially scanning the pixels of the panel row by row in response to the gate clock signal; and

a source driving circuit for generating a liquid crystal driving voltage corresponding to data in response to the gray voltage and the control signals, and for applying the generated liquid crystal driving voltage to the panel each of scanning,

wherein the source driving circuit generates a liquid crystal voltage having different values in high and low level intervals of the gate clock signal in response to the gray voltage.

2. The liquid crystal display claim 1, wherein said source driving circuit, while driving a positive polarity of the panel, generates a liquid crystal driving voltage having a first voltage level in a high-level interval of the gate clock signal, and generates a liquid crystal driving voltage having a second voltage level in a low-level interval of the gate clock signal, and

wherein both the first voltage level and the second voltage level are higher than a common voltage level, and the first driving voltage level is higher than of the second

driving voltage level.

3. The liquid crystal display of claim 2, wherein said source driving circuit, while driving a negative polarity of the panel, generates a liquid crystal driving voltage having a third voltage level in a high-level interval of the gate clock signal, and generates a liquid crystal driving voltage having a fourth voltage level in a low-level interval of the gate clock signal, and

wherein both the first voltage level and the second voltage level are lower than the common voltage level, and the third driving voltage level is lower than the fourth driving voltage level.

4. The liquid crystal display of claim 1, wherein said gray voltage generation circuit comprises:

a clock generator for generating a plurality of clock signals having a same period as the gate clock signal, in response to the gate clock signal;

a voltage generator for dividing a power supply voltage of the source driving circuit to a predetermined ratio to generate a plurality of voltages as reference for generating the gray voltage; and

a gray voltage generator for outputting the plural gray voltages to the source driving circuit, in response to the gate clock signals issued from said clock generator and the voltages generated by said voltage generator.

5. The liquid crystal display of claim 4, wherein the clock generator

comprises:

an input terminal for receiving the gate clock signal;

n-bit clock generation units coupled to the input terminal in parallel; and

n-bit output terminals each being coupled to said n-bit clock generation units,

wherein each of the clock generation units has a capacitor and a resister that are serially connected between the input terminal and the output terminal, and generates a clock signal having a same period as the gate clock signal.

6. The liquid crystal display of claim 4, wherein the voltage generator includes n-bit voltage generation units for dividing the power supply voltage to a predetermined ratio to generate the n-bit voltages each having different voltage level, and

wherein each of the voltage generation unit includes at least two and more resisters coupled between the power supply voltage and a ground voltage, and an output terminal coupled to one of contact points between the resisters.

7. The liquid crystal display of claim 4, wherein the gray voltage generator comprises:

a first gray voltage generation unit for generating (m/2)-bit gray voltages having a same polarity as the gate clock signal and each having different voltage level, so as to drive a positive polarity of the panel; and

a second gray voltage generation unit for generating (m/2)-bit gray voltages having a polarity opposite to the gate clock signal and each having different voltage

level, so as to drive a negative polarity of the panel.

8. The liquid crystal display of claim 7, wherein said first gray voltage generation unit includes at least one or more amplifier circuits having a first input terminal for receiving one of the n-bit clock signals from said clock generator and one of the n-bit reference voltages from said voltage generator, a second input terminal connected to a ground through a resister, and an amplifier circuit having a feedback resister connected between the second input terminal and the output terminal.

9. The liquid crystal display of claim 8, wherein the amplifier circuit adds the clock signal to the reference voltage, and amplifies the same to generate the gray voltage.

10. The liquid crystal display of claim 8, wherein the amplifier circuit further includes a resister for dividing the gray voltage, and an output terminal connected to the contact point of the resister, for outputting the divided gray voltage.

11. The liquid crystal display of claim 7, wherein said second gray voltage generation unit includes a first input terminal for receiving one of the n-bit reference voltages from said voltage generator, a second input terminal for receiving one of the n-bit clock signals from said clock generator, and an amplifier circuit having a feedback resister connected between the second input terminal and the output terminal.

12. The liquid crystal display of claim 11, wherein the amplifier circuit subtracts the clock signal from the reference voltage, and amplifies it to a predetermined ratio to generate the gray voltage.

13. The liquid crystal display of claim 11, wherein the amplifier circuit further includes a resister for dividing the gray voltage, and an output terminal connected to the contact point of the resister, for outputting the divided gray voltage.

14. A gray voltage generation circuit for a rapidly driving liquid crystal display comprising a liquid crystal panel having a plurality of pixels; a timing control circuit for generating a gate clock signal and a plurality of control signals; a gate driving circuit for sequentially scanning the pixels of the liquid crystal panel row by row in response to the gate clock signal; and a source driving circuit for generating a liquid crystal driving circuit corresponding to the data in response to a gray voltage and the control signals, and for applying the liquid crystal driving voltage to the panel each of scanning, said gray voltage generation circuit comprising:

a clock generator for generating a plurality of clock signals having a same period as the gate clock signal, in response to the gate clock signal;

a voltage generator for issuing a power supply voltage of the source driving circuit to a predetermined ratio to generate a plurality of voltages to be a reference for the gray voltage; and

a gray voltage generator for generating a plurality of gray voltages to the source driving circuit in response to the gate clock signals generated from said clock generator

and the voltages generated from said voltage generator.

15. The gray voltage generation circuit of claim 14, wherein said clock generator comprises:

an input terminal for receiving the gate clock signal;

n-bit clock generation units coupled to the input terminal in parallel; and

n-bit output terminals connected to each of said n-bit clock generation units,

wherein each of the clock generation units has a capacitor and a resister serially connected between the input terminal and the output terminal, and generates a clock signal having a same period as the gate clock signal.

16. The gray voltage generation circuit of claim 14, wherein the voltage generator includes n-bit voltage generation units for dividing the power supply voltage to a predetermined ratio to generate the n-bit voltages each having different voltage level, and

wherein each of the voltage generation units includes at least two and more resisters connected between the power supply voltage and a ground voltage, and an output terminal coupled to one of contact points between the resisters.

17. The gray voltage generation circuit of claim 14, wherein the gray voltage generator comprises:

a first gray voltage generation unit for generating (m/2)-bit gray voltages having a same polarity as the gate clock signal and each having different voltage level, so as to

drive a positive polarity of the panel; and

a second gray voltage generation unit for generating (m/2)-bit gray voltages having a polarity opposite to the gate clock signal and each having different voltage level, so as to drive a negative polarity of the panel.

18. The gray voltage generation circuit of claim 17, wherein said first gray voltage generation unit includes at least one or more amplifier circuits having a first input terminal for receiving one of the n-bit clock signals from said clock generator and one of the n-bit reference voltages from said voltage generator, a second input terminal connected to a ground through a resister, and an amplifier circuit having a feedback resister connected between the second input terminal and the output terminal.

19. The gray voltage generation circuit of claim 18, wherein the amplifier circuit adds the clock signal to the reference voltage, and amplifies the same to generate the gray voltage.

20. The gray voltage generation circuit of claim 18, wherein the amplifier circuit further includes a resister for dividing the gray voltage, and an output terminal connected to the contact point of the resisters, for outputting the divided gray voltage.

21. The gray voltage generation circuit of claim 17, wherein said second gray voltage generation unit includes a first input terminal for receiving one of the n-bit reference voltages from said voltage generator, a second input terminal for receiving

one of the n-bit clock signals from said clock generator, and an amplifier circuit having a feedback resister connected between the second input terminal and the output terminal.

22. The gray voltage generation circuit of claim 21, wherein the amplifier circuit subtracts the clock signal from the reference voltage, and amplifies it to a predetermined ratio to generate the gray voltage.

23. The gray voltage generation circuit claim 21, wherein the amplifier circuit further includes a resister for dividing the gray voltage, and an output terminal connected to the contact point of the resisters, for outputting the divided gray voltage.